

HYS25[L/S]256160A[F/C]-7.5
HYB25S256160AC
HYE25L256160AF

256MBit Mobile-RAM

Mobile-RAM

Commercial Temperature Range

Extended Temperature Range

Memory Products



N e v e r s t o p t h i n k i n g .

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all	Added new Product Type	

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Table of Contents		Page
1	Overview	6
1.1	Features	6
1.2	Description	6
2	Pin Configuration	8
3	Functional Description	11
3.1	Mode Register Definition	11
3.1.1	Operating Mode	11
3.2	Extended Mode Register	12
4	Electrical Characteristics	13
4.1	Operating Conditions	13
4.2	Current Specification	14
5	Package Outline	15



256MBit Mobile-RAM Mobile-RAM

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HYE25L256160AF

1 Overview

1.1 Features

- 16 Mbits × 16 organisation
- Fully synchronous to positive clock edge
- Four internal banks for concurrent operation
- Data mask (DM) for byte control with write and read data
- Programmable CAS latency: 2 or 3
- Programmable burst length: 1, 2, 4, 8, or full page
- Programmable wrap sequence: sequential or interleaved
- Random column address every clock cycle (1-N rule)
- Deep power down mode
- Extended mode register for Mobile-RAM features
- Temperature compensated self refresh with on-die temperature sensor
- Partial array self refresh
- Power down and clock suspend mode
- Automatic and controlled precharge command
- Auto refresh mode (CBR)
- 8192 refresh cycles / 64 ms
- Self-refresh with programmable refresh period
- Programmable power reduction feature by partial array activation during self-refresh
- $V_{DDQ} = 1.8V$ or $2.5 V$ or $3.3 V$
- $V_{DD} = 2.5 V$ or $3.3 V$
- P-TFBGA-54 package 9-by-6-ball array with 3 depopulated rows ($12 \times 8 \text{ mm}^2$)
- Operating temperature range:
commercial ($0 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)
extended ($-25 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Table 1 Performance ¹⁾

Part Number Speed Code			-7.5	Unit
max. Clock Frequency	@CL3	f_{CK3}	133	MHz
min. Clock Period	@CL3	t_{CK3}	7.5	ns
min. Access Time from Clock	@CL3	t_{AC3}	6.0	ns
min. Clock Period	@CL2	t_{CK2}	9.5	ns
min. Access Time from Clock	@CL2	t_{AC2}	6.0	ns

1) for $V_{DDQ} = 2.5 V$ or $3.3 V$;

1.2 Description

The 256MBit Mobile-RAM is a new generation of low power, four bank synchronous DRAM organized as 4 banks x 4 Mbit x 16 with additional features for mobile applications. The synchronous Mobile-RAM achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The device adds new features to the industry standards set for synchronous DRAM products. Parts of the memory array can be selected for Self-Refresh and the refresh period during Self-Refresh is programmable in 4 steps

which drastically reduces the self refresh current, depending on the case temperature of the components in the system application. In addition a “Deep Power Down Mode” is available. Operating the four memory banks in an interleave fashion allows random access operation to occur at higher rate. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

The Mobile-RAM is housed in a FBGA “chip-size” package. The Mobile-RAM is available in the commercial ($0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$) and extended ($-25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) temperature range.

Table 2 Ordering Information for Non-Green Products

Product Type ¹⁾	Function Code	Case Temperature Range	Package
HYB25L256160AC-7.5	PC133-333-522	commercial ($0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$)	P-TFBGA-54
HYB25S256160AC-7.5	PC133-333-522	commercial ($0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$)	P-TFBGA-54

Table 3 Ordering Information for Green Products



Product Type ¹⁾	Function Code	Case Temperature Range	Package
HYB25L256160AF-7.5	PC133-333-522	commercial ($0\text{ }^{\circ}\text{C} \leq \text{TC} \leq 70\text{ }^{\circ}\text{C}$)	P-TFBGA-54
HYE25L256160AF-7.5	PC133-333-522	extended ($-25\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)	P-TFBGA-54

- 1) HYB/E: designator for memory components for commercial /extended temperature range
 25L: Mobile-RAM at $V_{DD} = 2.5\text{ V}$
 256: 256-Mbit density
 160: Product variation x16
 A: Die revision A
 F/C: Lead & Halogen free / Lead-Containing
 -7.5: speed grade - see [Table 1](#)

2 Pin Configuration

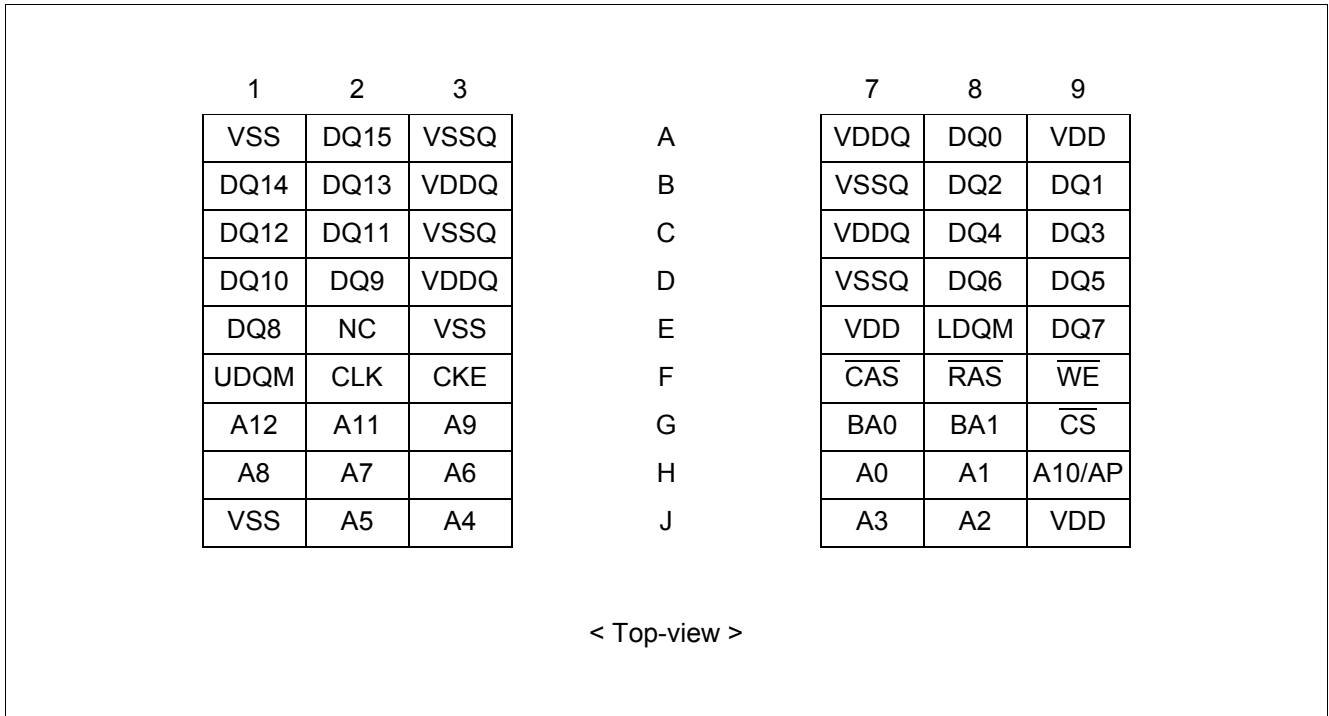


Figure 1 Pin Configuration P-TFBGA-54 (16 Mb × 16)

Table 4 Input/Output Signals

Pin	Symbol	Type	Polarity	Function			
F2	CLK	Input	Positive Edge	Clock			
F3	CKE	Input	Active High	Clock Enable			
G9	$\overline{\text{CS}}$	Input	Active Low	Chip Select			
F8	$\overline{\text{RAS}}$	Input	Active Low	Command Inputs			
F7	$\overline{\text{CAS}}$						
F9	$\overline{\text{WE}}$						
G8	BA1	Input	Active High	Bank Address Inputs			
G7	BA0						
G1	A12	Input	Active High	Address Inputs			
G2	A11						
H9	A10/AP						
G3	A9						
H1	A8						
H2	A7						
H3	A6						
J2	A5						
J3	A4						
J7	A3						
J8	A2						
H8	A1						
H7	A0						
A2	DQ15				Input/Output	Active High	Data Input/Output
B1	DQ14						
B2	DQ13						
C1	DQ12						
C2	DQ11						
D1	DQ10						
D2	DQ9						
E1	DQ8						
E9	DQ7						
D8	DQ6						
D9	DQ5						
C8	DQ4						
C9	DQ3						
B8	DQ2						
B9	DQ1						
A8	DQ0						
F1	UDQM	Input	Active High	Data Input/Output Mask			
E8	LDQM						

Pin Configuration

Table 4 Input/Output Signals (cont'd)

Pin	Symbol	Type	Polarity	Function
E2	NC	–	–	Not Connected
A7, B3, C7, D3	V_{DDQ}	Supply	–	DQ Power Supply
A3 B7 C3 D7	V_{SSQ}	Supply	–	DQ Ground
A9 E4 J9	V_{DD}	Supply	–	Power Supply
A1 E3 J1	V_{SS}	Supply	–	Ground

3 Functional Description

3.1 Mode Register Definition

MR

Mode Register Definition

(BA[1:0] = 00_B)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	MODE						CL		BT	BL			
reg. addr		w						w		w	w			

Field	Bits	Type	Description
BL	[2:0]	w	Burst Length Number of sequential bits per DQ related to one read/write command; <i>Note: All other bit combinations are RESERVED.</i> 000 1 001 2 010 4 011 8 111 full page (sequential burst type only)
BT	3	w	Burst Type 0 Sequential 1 Interleaved
CL	[6:4]	w	CAS Latency Number of full clocks from read command to first data valid window; <i>Note: All other bit combinations are RESERVED.</i> 010 2 011 3
MODE	[12:7]	w	Operating Mode <i>Note: All other bit combinations are RESERVED.</i> 000000 Burst Read/Burst Write 000100 Burst Read/Single Write

3.1.1 Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A12-A7 set to zero, and bits A6-A0 set to the desired values. Burst Length for Write bursts is fixed to one by issuing a Mode Register Set command with bits A12-A10 and A8-A7 each set to zero, bit A9 set to one, and bits A0-A6 set to the desired values.

All other combinations of values for A12-A7 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

3.2 Extended Mode Register

EMR

Extended Mode Register Definition

(BA[1:0] = 10_B)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	MODE									TCSR		PASR	
reg. addr		w									w		w	

Field	Bits	Type	Description ¹⁾
PASR	[2:0]	w	Partial Array Self Refresh 000 banks to be self refreshed: all 4 of 4 001 banks to be self refreshed: 2 of 4, BA[1:0] = 00 _B or 01 _B 010 banks to be self refreshed: 1 of 4, BA[1:0] = 00 _B 101 banks to be self refreshed: 0.5 of 4, BA[1:0] = 00 _B & RA12 = 0 _B 110 banks to be self refreshed: 0.25 of 4, BA[1:0] = 00 _B & RA[12:11] = 00 _B
TCSR	[4:3]	w	Temperature Compensated Self Refresh 00 on-chip temperature sensor enabled 01 Maximum case temperature: 45°C, on-chip temperature sensor disabled 10 Maximum case temperature: 15°C, on-chip temperature sensor disabled 11 Maximum case temperature: 85°C, on-chip temperature sensor disabled
MODE	[12:5]	w	Operating Mode 00h Normal operation

1) All other bit combinations are RESERVED.

4 Electrical Characteristics

4.1 Operating Conditions

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	-1.0	—	$V_{DD} + 0.5$	V	—
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	-1.0	—	+4.6	V	—
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-1.0	—	+4.6	V	—
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-1.0	—	+4.6	V	—
Operating Case Temperature (extended)	T_{CASE}	-25	—	+85	°C	—
Storage Temperature (Plastic)	T_{STG}	-55	—	+150	°C	—
Power Dissipation	P_D	—	—	0.7	W	—
Short Circuit Output Current	I_{OUT}	—	50	—	mA	—

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 6 Recommended Operating Conditions and DC Characteristics¹⁾

Parameter	Symbol	Values		Unit	Note/ Test Condition
		min.	max.		
Supply Voltage	V_{DD}	+2.3	+3.6	V	—
I/O Supply Voltage	V_{DDQ}	+1.65	+3.6	V	2)
Supply Voltage	V_{SS}	0	0	V	—
I/O Supply Voltage	V_{SSQ}	0	0	V	—
Input High (Logic 1) Voltage	V_{IH}	$0.8 \times V_{DDQ}$	$V_{DDQ} + 0.3$	V	3)4)
Input Low (Logic 0) Voltage	V_{IL}	-0.3	+0.3	V	3)4)
Output High (Logic 1) Voltage	V_{OH}	$V_{DDQ} - 0.2$	—	V	$I_{OH} = -0.1$ mA
Output Low (Logic 0) Voltage	V_{OL}	—	+0.2	V	$I_{OH} = +0.1$ mA
Input Leakage Current	I_{IL}	-5	+5	μA	Any input $0 \text{ V} \leq V_{IN} \leq V_{DD}$; all other pins not under test $V_{IN} = 0 \text{ V}$
Output Leakage Current	I_{OZ}	-5	+5	μA	DQ is disabled; $0 \text{ V} \leq V_{OUT} \leq V_{DDQ}$

1) $0 \text{ °C} \leq T_C \leq 70 \text{ °C}$ (comm.) and $-25 \text{ °C} \leq T_{CASE} \leq +85 \text{ °C}$

2) $V_{DDQ} < V_{DD} + 0.3 \text{ V}$

3) All voltages referenced to V_{SS}

4) V_{IH} may overshoot to $V_{DDQ} + 2.0 \text{ V}$ for pulse width of $< 4 \text{ ns}$.

V_{IL} may undershoot to -2.0 V for pulse width $< 4 \text{ ns}$.

Pulse width measured at 50% points with amplitude measured peak to DC reference

Table 7 Input and Output Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Input Capacitance: CLK	C_{I1}	–	–	3.5	pF	1)
Input Capacitance: All other input-only pins	C_{I2}	–	–	3.8	pF	1)
Input/Output Capacitance: DQ	C_{I0}	4.0	–	5.0	pF	1)

1) These values are guaranteed by design and are tested on a sample base only. $V_{DDQ} = V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $f = 1 \text{ MHz}$, $T_{CASE} = 25 \text{ }^\circ\text{C}$, $V_{OUT(DC)} = V_{DDQ}/2$, V_{OUT} (Peak to Peak) 0.2 V. Unused pins are tied to ground.

4.2 Current Specification

Table 8 I_{DD} Specification and Conditions¹⁾²⁾

Parameter	Symbol	–7.5		Unit	Note/ Test Condition
		typ.	max.		
Operating current Single bank access cycles	I_{DD1}	—	65	mA	$t_{RC} = t_{RC,MIN}$ ³⁾
Precharge standby current Power down mode	I_{DD2P}	—	0.6	mA	$\overline{CS} = V_{IH,MIN}$, $CKE \leq V_{IL,MAX}$ ³⁾
Precharge standby current Non power down mode	I_{DD2N}	—	20	mA	$\overline{CS} = V_{IH,MIN}$, $CKE \geq V_{IH,MIN}$ ³⁾
Non operating current Active state of 1 upto 4 banks, power down	I_{DD3P}	—	3.5	mA	$\overline{CS} = V_{IH,MIN}$, $CKE \leq V_{IL,MAX}$ ³⁾
Non operating current Active state of 1 upto 4 banks, non power down	I_{DD3N}	—	25	mA	$\overline{CS} = V_{IH,MIN}$, $CKE \geq V_{IH,MIN}$ ³⁾
Burst operating current Read command cycling	I_{DD4}	—	80	mA	³⁾⁴⁾
Auto refresh current Auto refresh command cycling	I_{DD5}	—	155	mA	$t_{RC} = t_{RC,MIN}$
Self refresh current	I_{DD6}			μA	$t_{CK} = \text{infinity}$, $CKE = 0.2 \text{ V}$
Deep power down mode current	I_{DD7}	—	5	μA	

1) $0 \text{ }^\circ\text{C} \leq T_C \leq 70 \text{ }^\circ\text{C}$ (comm.) and $-25 \text{ }^\circ\text{C} \leq T_{CASE} \leq +85 \text{ }^\circ\text{C}$; recommended operating conditions unless otherwise noted

2) For proper power-up see the operation section of this data sheet.

3) These parameters depend on the frequency. These values are measured at 133MHz for –7.5 and at 100MHz for –8 parts. Input signals are changed once during t_{CK} . If the devices are operating at a frequency less than the maximum operation frequency, these current values are reduced.

4) These parameters are measured with continuous data stream during read access and all DQs toggling. CL = 3 and BL = 4 is used and the V_{DDQ} current is excluded.

5 Package Outline

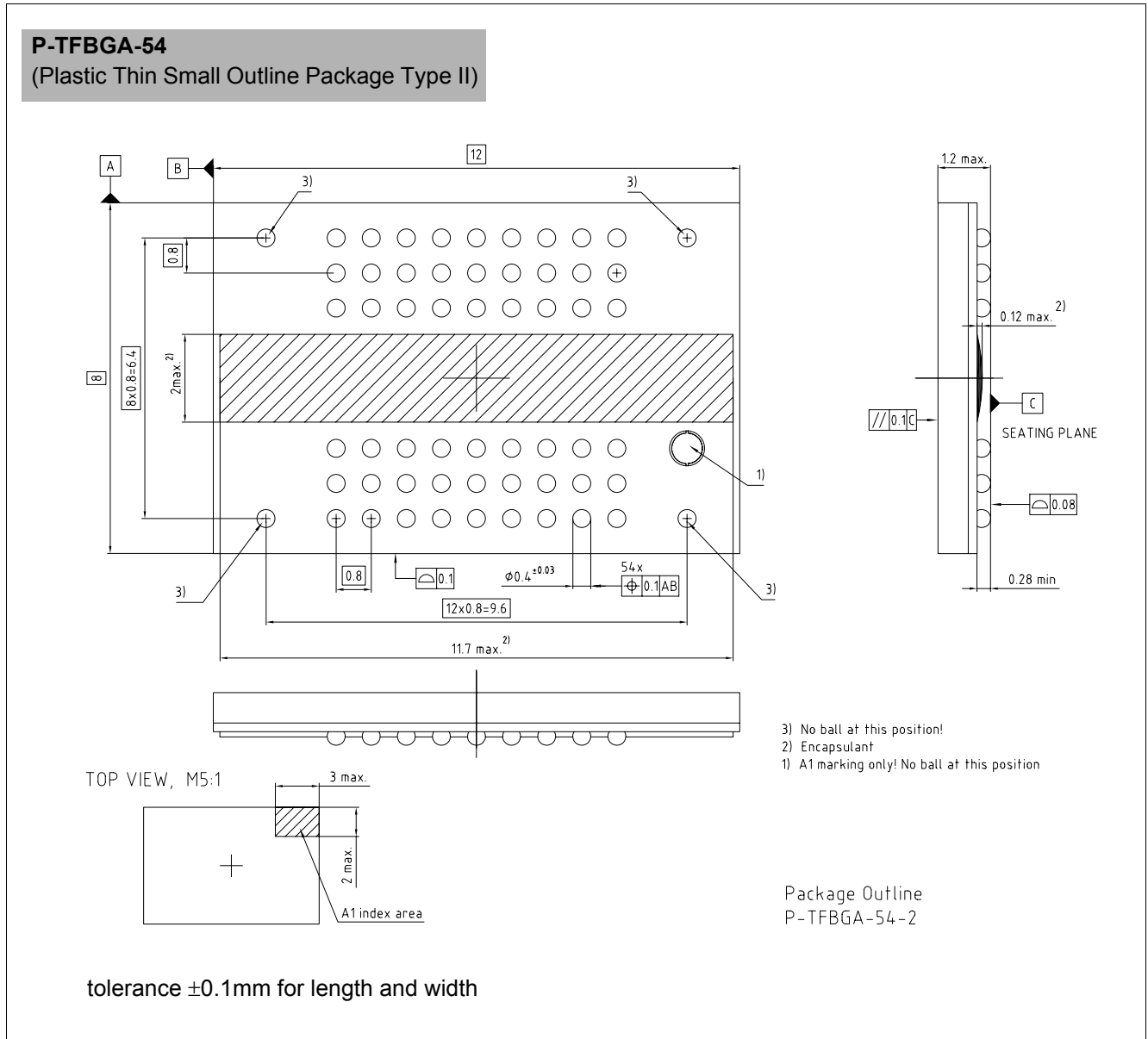


Figure 2 Package Outline

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SMD = Surface Mounted Device

Dimensions in mm

<http://www.infineon.com>